CLAIMS

What is claimed is:

1. A method for providing an area optimized binary orthogonality checker for a scalable selector system for controlling data transfers and routing in a data processing system comprising the steps of:

determining the gate count for an implementation of an orthogonality checker, and

minimizing the gate count and area needed to implement an orthogonality checker given a library of logical gates to implement the circuit and the area for each gate in the library.

2. The method according to claim 1 including a steps of:

determining the optimal mix of hierarchical level, and

determining the inputs to implement a given orthogonality checker to achieve the minimized circuit.

[0030] 3. The method according to claim 1, where the area of a binary orthogonality checker is implemented in a static CMOS circuits by minimizing the gate count and area needed for checker implementation given a library of logical gates to implement the circuit and the area for each gate in the library,.

[0031] 4. The method according to claim 3, including a step of determining an optimal mix of hierarchical levels and inputs to implement a given orthogonality checker to achieve the minimized circuit.

[0032] 5. The method according to claim 4 wherein said orthogonality checker is employed in a scalable selector system for controlling data transfers and routing in a data processing system, comprising a plurality of input data buses coupled to a multiple-

bit, multiple bus selector having data, data valid, and an orthogonality check outputs and having multiple data input bus ports coupled for receipt of signal from said plurality of input data buses.

[0033] 6. The method according to claim 5 wherein after determining an expected number for the gate count for an implementation of an orthogonality checker, and the binary orthogonality checking is provided by hierarchically combining the checks with smaller numbers of inputs and performing the total check of a large number of inputs with less gates and in a smaller area

[0034] 7. The method according to claim 1 wherein after determining an expected number for the gate count, multiple checks with reduced input sets are combined into one larger check and the orthogonality checking is performed, with a check on each input set, as well as combining an OR of all the inputs to the check.

[0035] 8. The method according to claim 7 wherein the resulting OR values are then checked for orthogonality, and the results of all the checks are ORed together.

[0036] 9. The method according to claim 8 wherein the structure for orthogonality check is extended to multiple hierarchical levels and works with orthogonality checks said extended size of implementation.

10. The method according to claim 9 wherein the structure determined is an optimal hierarchical structure for a given technology library and a given number of inputs to check..

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